

CLAIMS:

1. A method of forming timing parameters for a circuit design having a predefined routing topology within an integrated circuit, the method comprising:

determining sets of timing attributes for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the integrated circuit in which the circuit design may be placed;

forming timing parameters in response to the sets of timing attributes; and

associating the timing parameters with the routing topology.

2. The method of claim 1, wherein the routing topology comprises a source and at least one sink, and wherein each set of timing attributes comprises a signal delay between each source-sink pair.

3. The method of claim 2, wherein the forming timing parameters comprises:

selecting a minimum delay in response to the signal delay for each source-sink pair in each set of timing attributes; and

selecting a maximum delay in response to the signal delay for each source-sink pair in each set of timing attributes.

4. The method of claim 3, wherein the source provides a clock signal to the at least one sink and wherein each set of timing attributes further comprises a clock skew for each source-sink pair.

5. The method of claim 4, wherein the forming further comprises selecting a maximum skew in response to the clock skew for each source-sink pair in each set of timing attributes.

6. The method of claim 1, wherein the integrated circuit is a programmable logic device, and where each of the plurality of locations is defined by a group of programmable logic blocks.

7. The method of claim 6, wherein the circuit design comprises at least one clock net.

8. A method of analyzing timing of a circuit design associated with a template having a predefined routing topology within an integrated circuit, the method comprising:

determining sets of timing attributes for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the integrated circuit in which the template may be applied;

forming timing parameters in response to the sets of timing attributes;

associating the timing parameters with the routing topology;

placing and routing the circuit design within the integrated circuit based on the template; and

analyzing the circuit design using the timing parameters.

9. The method of claim 8, wherein the routing topology comprises a source and at least one sink, and wherein each set of timing attributes comprises a signal delay between each source-sink pair.

10. The method of claim 9, wherein the forming timing parameters comprises:

selecting a minimum delay in response to the signal delay for each source-sink pair in each set of timing attributes; and

selecting a maximum delay in response to the signal delay for each source-sink pair in each set of timing attributes.

11. The method of claim 10, wherein the source provides a clock signal to the at least one sink and wherein each set of timing attributes further comprises a clock skew for each source-sink pair.

12. The method of claim 11, wherein the forming further comprises selecting a maximum skew in response to the clock skew for each source-sink pair in each set of timing attributes.

13. The method of claim 8, wherein the integrated circuit is a programmable logic device, and where each of the plurality of locations is defined by a group of programmable logic blocks.

14. The method of claim 13, wherein the circuit design comprises at least one clock net.

15. An apparatus for forming timing parameters for a circuit design associated with a template having a predefined routing topology within an integrated circuit, the apparatus comprising:

means for determining sets of timing attributes for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the integrated circuit in which the template may be applied; and

means for forming timing parameters in response to the sets of timing attributes.

16. The apparatus of claim 15, further comprising:

means for placing and routing the circuit design within the integrated circuit based on the template; and

means for analyzing the circuit design using the timing parameters.

17. A computer readable medium having stored thereon instructions that, when executed by a processor, cause the processor to perform a method of forming timing parameters for a circuit design associated with a template having a predefined routing topology within an integrated circuit, the method comprising:

determining sets of timing attributes for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the integrated circuit in which the template may be applied;

forming timing parameters in response to the sets of timing attributes; and

associating the timing parameters with the routing topology.

18. The computer readable medium of claim 17, further comprising:

placing and routing the circuit design within the integrated circuit based on the template; and

analyzing the circuit design using the timing parameters.

19. A system for forming timing parameters for a circuit design associated with a template having a predefined routing topology within an integrated circuit, the system comprising:

a processing unit having access to one or more storage

devices;

at least a portion of the one or more storage devices having a program product configured to:

determine sets of timing attributes for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the integrated circuit in which the template may be applied;

form timing parameters in response to the sets of timing attributes; and

associate the timing parameters with the routing topology.

20. The system of claim 19, wherein the program product is further configured to:

place and route the circuit design within the integrated circuit based on the template; and

analyze the circuit design using the timing parameters.